IN THE CLAIMS:

Please substitute the following claims for the same-numbered claims in the application:

1. (Current Amended) A method of manufacturing integrated circuit chips comprising:

providing a supporting wafer comprising oxide regions in a substrate and having a planar surface ~~and oxide regions at said planar surface~~ at which said oxide regions and said substrate are exposed;

partially joining an integrated circuit wafer to said planar surface of said supporting wafer at a limited number of joining points ~~corresponding to said oxide regions~~ such that said oxide regions bond with said integrated circuit wafer to form said joining points and said substrate does not bond with but maintains contact with said integrated circuit wafer so as to support said integrated circuit wafer during subsequent processing and cutting;

processing said integrated circuit wafer to form devices and wiring in said integrated circuit wafer; and

cutting through said integrated circuit wafer to form chip sections,

wherein, during said cutting process, said integrated circuit wafer separates from said supporting wafer in chip sections where said integrated circuit wafer is not joined to said supporting wafer by said joining points.

2. (Original) The method in claim 1, further comprising aligning said integrated circuit wafer to said supporting wafer before performing said joining process.

3. (Original) The method in claim 1, further comprising, before said joining process, roughening portions of said integrated circuit wafer facing said supporting wafer to create

rough surface portions at the interface of said integrated circuit wafer, wherein said roughening process avoids producing rough surface portions adjacent said joining points.

4. (Original) The method in claim 1, wherein chip sections where said integrated circuit wafer remains joined to said supporting wafer are thicker than said chips sections where said integrated circuit wafer separates from said supporting wafer.

5. (Original) The method in claim 1, wherein said joining process comprises a bonding process.

6. (Original) The method in claim 1, wherein said joining process comprises a thermal oxide bonding process.

7. (Original) The method in claim 1, wherein said joining process creates said joining points to survive processing temperatures that are reached during said processing that forms said devices and said wiring in said integrated circuit wafer.

8. (Currently Amended) A method of manufacturing integrated circuit chips comprising:

providing a supporting wafer comprising oxide regions in a substrate and having a planar surface ~~and oxide regions at said planar surface~~ at which said oxide regions and said substrate are exposed;;

partially joining an integrated circuit wafer to said planar surface of said supporting wafer at a limited number of joining points ~~corresponding to said oxide regions~~ such that said oxide regions bond with said integrated circuit wafer to form said joining points and said substrate does not bond with but maintains contact with said integrated circuit wafer so as to support said integrated circuit wafer during subsequent reducing, processing and cutting;

reducing the thickness of said integrated circuit wafer;

processing said integrated circuit wafer to form devices and wiring in said integrated circuit wafer; and

cutting through said integrated circuit wafer to form chip sections,

wherein, during said cutting process, said integrated circuit wafer separates from said supporting wafer in chip sections where said integrated circuit wafer is not joined to said supporting wafer by said joining points.

9. (Original) The method in claim 8, further comprising aligning said integrated circuit wafer to said supporting wafer before performing said joining process.

10. (Original) The method in claim 8, further comprising, before said joining process, roughening portions of said integrated circuit wafer facing said supporting wafer to create rough surface portions at the interface of said integrated circuit wafer, wherein said roughening process avoids producing rough surface portions adjacent said joining points.

11. (Original) The method in claim 8, wherein chip sections where said integrated circuit wafer remains joined to said supporting wafer are thicker than said chips sections where said integrated circuit wafer separates from said supporting wafer.

12. (Original) The method in claim 8, wherein said joining process comprises a bonding process.

13. (Original) The method in claim 8, wherein said joining process comprises a thermal oxide bonding process.

14. (Original) The method in claim 8, wherein said joining process creates said joining points to survive processing temperatures that are reached during said processing that forms said devices and said wiring in said integrated circuit wafer.

15. (Currently Amended) A method of manufacturing integrated circuit chips comprising:

providing a supporting wafer comprising oxide regions in a substrate and having a planar surface ~~and oxide regions at said planar surface~~ at which said oxide regions and said substrate are exposed;

partially joining an integrated circuit wafer to said planar surface of said supporting wafer at a limited number of joining points ~~corresponding to said oxide regions~~ such that said oxide regions bond with said integrated circuit wafer to form said joining points and said substrate does not bond with but maintains contact with said integrated circuit wafer so as to support said integrated circuit wafer during subsequent polishing, processing and cutting;

chemically-mechanically polishing said integrated circuit wafer to reduce the thickness of said integrated circuit wafer;

processing said integrated circuit wafer to form devices and wiring in said integrated circuit wafer; and

cutting through said integrated circuit wafer to form chip sections,

wherein, during said cutting process, said integrated circuit wafer separates from said supporting wafer in chip sections where said integrated circuit wafer is not joined to said supporting wafer by said joining points.

16. (Original) The method in claim 15, further comprising aligning said integrated circuit wafer to said supporting wafer before performing said joining process.

17. (Original) The method in claim 15, further comprising, before said joining process, roughening portions of said integrated circuit wafer facing said supporting wafer to create rough surface portions at the interface of said integrated circuit wafer, wherein

said roughening process avoids producing rough surface portions adjacent said joining points.

18. (Original) The method in claim 15, wherein chip sections where said integrated circuit wafer remains joined to said supporting wafer are thicker than said chips sections where said integrated circuit wafer separates from said supporting wafer.

19. (Original) The method in claim 15, wherein said joining process comprises a bonding process.

20. (Original) The method in claim 15, wherein said joining process comprises a thermal oxide bonding process.

21. (New) The method in claim 1, wherein said cutting process comprises cutting through said integrated circuit wafer without cutting through said support wafer.

22. (New) The method in claim 21, wherein said cutting process comprises using a laser to cut through said integrated circuit wafer.

23. (New) The method in claim 8, wherein said cutting process comprises cutting through said integrated circuit wafer without cutting through said support wafer.

24. (New) The method in claim 23, wherein said cutting process further comprises using a laser to cut through said integrated circuit wafer without cutting through said support wafer.

25. (New) The method in claim 24, wherein said cutting process comprises cutting through said integrated circuit wafer without cutting through said support wafer.

26. (New) The method in claim 25, wherein said cutting process further comprises using a laser to cut through said integrated circuit wafer without cutting through said support wafer.